82. (Amended) The apparatus of claim 74 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed over said semiconductor layer.

83. (Amended) The apparatus of claim 75 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed over said semiconductor layer.

84. (Amended) The apparatus of claim 76 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed over said semiconductor layer.

85. (Amended) The apparatus of claim 77 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed over said semiconductor layer.

REMARKS

At the outset, the Primary Examiner is thanked for her review and consideration of the present application.

The Examiner's Final Office Action dated April 24, 2001 has been received and its contents carefully noted. Claims 16-20, 24, 25, 56-61 and 74-91 are pending in the present application, of which 16, 21, 26, 32, 38, 44, 50, 56, 62, 68, 74, 75, 76, and 77 are independent. By this amendment, claims 16, 17, 19, 20, 56, 57, 58, 60, 74, 75, 76, 77, 80, 81, and 82-85 have been amended.

Claims 16-20, 24, 25 , 80, and 86 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Begin et al., in view of Miyachi et al., Nakayama et al., and Kawasaki et al., further in view of Codama et al., of record, further in view of Presley (U.S. Patent No. 4,475,027), further in view of Kawachi et al., the newly cited article entitled "Large-Area Process for Fabrication of Poly-Si Thin Film Transistors Using Bucket Ion Source and XeCl Excimer Laser Annealing."

Claims 56-61, 81 and 87 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Begin et al., in view of Miyachi et al., Nakayama et al., and Kawasaki et al., further in view of Codama et al., all of record, further in view of Hashizume (JP 03-286518),

further in view of Kawachi et al., the newly cited article entitled "Large-Area Process for Fabrication of Poly-Si Thin Film Transistors Using Bucket Ion Source and XeCl Excimer Laser Annealing."

Claims 74-79, 82-85, and 89-91 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Begin et al., in view of Miyachi et al., Nakayama et al., and Kawasaki et al., further in view of Codama et al., all of record, further in view of Kawachi et al., the newly cited article entitled "Large-Area Process for Fabrication of Poly-Si Thin Film Transistors Using Bucket Ion Source and XeCl Excimer Laser Annealing."

The above-summarized rejections are respectfully traversed at least for the reasons provided below.

The apparatus of the present invention includes, among other things, a vacuum chamber, an ion-introducing apparatus, and a light processing apparatus. The light processing chamber of the light processing apparatus is connected to the ion introducing apparatus through the vacuum chamber.

In use, a dopant impurity is doped into a semiconductor layer provided over a substrate in the ion-introducing apparatus. Thereafter, the semiconductor is irradiated with a light such as a laser light and an infrared light in the light processing chamber.

In the present invention, the vacuum chamber is provided with a mechanism for transporting the substrate provided with the semiconductor layer thereover from the ion introducing apparatus to the light processing chamber without exposing the substrate to the air.

Because the substrate provided with the semiconductor layer thereover is transported without exposing the substrate to the air, the semiconductor layer is prevented from being polluted by the air and external impurity. Therefore, when the semiconductor layer is doped with the dopant impurity and is prevented from being doped with various impurities from the air and external impurity.

In the light processing chamber, a light such as a laser light with an infrared light is irradiated onto the semiconductor layer to activate the dopant impurity doped into the semiconductor layer.

Because the light, such as the laser and the infrared light, is radiated onto the semiconductor layer free from various impurity from the air and external impurity, the semiconductor layer is prevented from being influenced by the various impurity from the air and external impurity.

Therefore, a conductivity of a part of the semiconductor layer doped with the dopant impurity is prevented from being influenced by various impurity from the air and external impurity. That is, the present invention is suitable for improving the control of the conductivity of the part of the semiconductor layer doped with the dopant impurity.

Applicants respectfully submit that the cited prior art references, applied separately or in combination, fail to teach, disclose, or suggest Applicants' invention as recited in the pending claims. As set forth above, using Applicants' claimed invention, improved control of conductivity of a doped region of a semiconductor layer is achieved.

It is well-established that, in order to show obviousness, all limitations in the claim must be taught or suggested by the prior art. In Re Boyka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); MPEP § 2143.03. It is error to ignore specific limitations distinguishing over the references. In Re Boe, 184 U.S.P.Q. 38, 505 F.2d 1297 (C.C.P.A. 1974); In Re Saether, 181 U.S.P.Q. 36, 492 F.2d 849 (C.C.P.A. 1974); In Re Glass, 176 U.S.P.Q. 489, 472 F.2d 1388 (C.C.P.A. 1973).

Citing references which merely indicate that isolated elements and/or features recited in the claims are known is not a sufficient basis for concluding that the combination of claimed elements would have been obvious. Ex parte Hiyamizu 10 USPQ2d 1393 (BPAI 1988).

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In re Geiger 815 F2d 686 (Fed. Cir. 1987), 2 USPQ2d 1276.

Applicants note that the burden of establishing a prima facie case of obviousness under § 103 lies with the Patent Office. In re Fine, 5 USPQ2d 1596 (Fed. Cir. 1988). To establish a prima facie case of obviousness, there must be (1) some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art)

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to modify the reference or to combine reference teachings to achieve the claimed invention and (2) the prior art must teach or suggest all the claim limitations. MPEP § 2143. Also, simply because the references could be combined does not mean that they should be. MPEP § 2143.01, citing In re Mills, 16 USPQ2d 1430 (Fed. Cir. 1990).

As set forth in the arguments above, the Office has not met both requirements 1 and 2, and a prima facie case of obviousness has not been established.

Claims 16, 17, 19, 20, 56, 57, 58, 60, 74, 75, 76, 77, 80, 81, and 82-85 have been amended to further clarify the claim language.

In view of the amendment and arguments set forth above, the § 103 rejections of claims 16-20, 24, 25, 56-61, and 74-91 are respectfully requested to be reconsidered and withdrawn.

CONCLUSION

Having responded to all rejections set forth in the outstanding Final Office Action, it is submitted that claims 16-20, 24, 25, 56-61 and 74-91 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Primary Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Primary Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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VERSION OF AMENDED CLAIMS
SHOWING CHANGES MADE

16. (Amended) An apparatus for processing a semiconductor [provided on a substrate] comprising:

a vacuum chamber;

an ion introducing apparatus connected to said vacuum chamber for doping a semiconductor layer formed [on] over a substrate with a dopant impurity;

a laser processing apparatus comprising a laser processing chamber and a laser for treating said semiconductor layer with a laser light in said laser processing chamber after said doping, said laser processing chamber connected to said ion introducing apparatus through said vacuum chamber [for treating said semiconductor layer with a laser light after said doping]; and

a mechanism provided to said vacuum chamber for transporting said substrate from said ion introducing apparatus to said laser processing [apparatus] chamber without exposing said substrate to the air,

[said laser processing apparatus comprising a chamber and a laser wherein a rectangular-shaped laser beam having an elongated cross-section irradiates said semiconductor layer,]

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

17. (Amended) The apparatus of claim 16 wherein said laser is placed outside said laser processing chamber, said laser processing chamber having a window through which said [rectangular shaped] laser [beam] light [having an elongated cross section] is introduced into said laser processing chamber.

19. (Amended) The apparatus of claim 16 further comprising a chamber, connected with said [preliminary] vacuum chamber, for introduction and takeout of said substrate.

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20. (Amended) The apparatus of claim 17 wherein said laser light is rectangular-shaped on a surface of said semiconductor film, and [the chamber of] said laser processing [apparatus] chamber is provided with a mechanism for moving said substrate in a direction orthogonal to [the elongation] a longitudinal direction of said laser [beam] light in order that a whole surface of said substrate is scanned with said laser [beam] light.

56. (Amended) An apparatus for processing a semiconductor [provided on a substrate] comprising:

a vacuum chamber;

an ion introducing apparatus connected to said vacuum chamber for doping a semiconductor layer formed [on] over a [substantially square] substrate with a dopant impurity;

a laser processing apparatus comprising a laser processing chamber and a laser for treating said semiconductor layer with a rectangular shaped laser light in said laser processing chamber after said doping, said laser processing chamber connected to said ion introducing apparatus through said vacuum chamber [for treating said semiconductor layer with a laser light after said doping]; and

a mechanism provided to said vacuum chamber for transporting said [substantially square] substrate from said ion introducing apparatus to said laser processing [apparatus] chamber without exposing said [substantially square] substrate to the air,

[said laser processing apparatus comprising a chamber and a laser wherein a rectangular-shaped laser beam having an elongated cross-section irradiates said semiconductor layer and wherein] said rectangular-shaped laser [beam] light has a length greater than a width of said [substantially square] substrate,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

57. (Amended) The apparatus of claim 56, wherein said [substantially square] substrate is glass.

58. (Amended) The apparatus of claim 56 wherein said [substantially square] substrate is 300 mm. x 400 mm and said rectangular-shaped laser [beam] light is 2 mm x 350 mm.

60. (Amended) The apparatus of claim 56 wherein said laser processing apparatus further comprises a sample holder for moving said substrate in a direction orthogonal to said rectangular-shaped laser [beam] light.

74. (Amended) An apparatus for [processing] forming a semiconductor device [provided on a substrate] comprising:

a vacuum chamber;

an ion introducing apparatus connected with said vacuum chamber for doping a semiconductor layer formed [on] over a substrate with a dopant impurity;

a laser processing apparatus comprising a laser processing chamber and a laser for treating said semiconductor layer with a laser light in said laser processing chamber after said doping, said laser processing chamber connected to said ion introducing apparatus through said vacuum chamber [for treating said semiconductor layer with a laser light after said doping]; and

a mechanism provided to said vacuum chamber for transporting said substrate from said ion introducing apparatus to said laser processing [apparatus] chamber without exposing said substrate to the air,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

75. (Amended) An apparatus for processing a semiconductor [provided on a substrate] comprising:

a vacuum chamber;

an ion introducing apparatus connected with said vacuum chamber for doping a semiconductor layer formed [on] over a substrate with a dopant impurity;

a light processing apparatus comprising a light processing chamber and a light source chamber for treating said semiconductor layer with an infrared light in said light processing chamber after said doping, said light processing chamber connected to said ion introducing apparatus through said vacuum chamber [for treating said semiconductor layer with an infrared light after said doping]; and

a mechanism provided to said vacuum chamber for transporting said substrate from said ion introducing apparatus to said light processing [apparatus] chamber without exposing said substrate to the air,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

76. (Amended) An apparatus for processing a semiconductor [provided on a substrate] comprising:

a vacuum chamber;

an ion introducing apparatus connected with said vacuum chamber for doping a semiconductor layer formed [on] over a substrate with a dopant impurity;

a light processing apparatus comprising a light processing chamber and a light source chamber for irradiating an infrared light to a part of said semiconductor layer doped with said dopant impurity, the irradiation of said infrared light conducted in said light processing chamber, said light processing chamber connected to said ion introducing apparatus through said vacuum chamber [for irradiating an infrared light to a part of said semiconductor layer doped with said dopant impurity]; and

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a mechanism provided to said vacuum chamber for transporting said substrate from said ion introducing apparatus to said light processing [apparatus] chamber without exposing said substrate to the air,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

77. (Amended) An apparatus for processing a semiconductor [provided on a substrate] comprising:

a vacuum chamber;

an ion introducing apparatus connected with said vacuum chamber for doping a semiconductor layer formed [on] over a substrate with a dopant impurity;

a laser processing apparatus comprising a laser processing chamber and a laser for irradiating a laser light to a part of said semiconductor layer doped with said dopant impurity, the irradiation of said laser light conducted in said laser processing chamber, said laser processing chamber connected to said ion introducing apparatus through said vacuum chamber [for irradiating a laser light to a part of said semiconductor layer doped with said dopant impurity]; and

a mechanism provided to said vacuum chamber for transporting said substrate from said ion introducing apparatus to said laser processing [apparatus] chamber without exposing said substrate to the air,

said dopant impurity being made a plasma around a grid electrode of said ion introducing apparatus and being accelerated toward said semiconductor layer by a voltage applied to an anode electrode of said ion introducing apparatus.

80. (Amended) The apparatus of claim 16 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed [on] over said semiconductor layer.

81. (Amended) The apparatus of claim 56 wherein said semiconductor layer placed in

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said ion introducing apparatus has a silicon oxide layer formed [on] over said semiconductor layer.

82. (Amended) The apparatus of claim 74 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed [on] over said semiconductor layer.

83. (Amended) The apparatus of claim 75 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed [on] over said semiconductor layer.

84. (Amended) The apparatus of claim 76 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed [on] over said semiconductor layer.

85. (Amended) The apparatus of claim 77 wherein said semiconductor layer placed in said ion introducing apparatus has a silicon oxide layer formed [on] over said semiconductor layer.

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